AMENDMENTS TO THE SPECIFICATION

IN THE TITLE OF THE INVENTION:

Please amend the title as follows:

DATA DRIVEN TYPE INFORMATION PROCESSING APPARATUS HAVING DEADLOCK BREAKING FUNCTION

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 12, line 8 with the following new paragraph:

Now, the data packet used in one embodiment of the present invention is the data packet including the tag field (destination node number field F1, generation number field F2, instruction code filed F3) and data field (data field F4) shown in Fig. 5, additionally having the host transfer flag. An example, in which the data transmission apparatus of Fig. 1 is applied to the data driven type information ~~procesisng~~ processing apparatus PE described with reference to Fig. 10 above, will be described in the following.

Please replace the paragraph beginning at page 12, line 20 with the following new paragraph:

Referring to Fig. 2, the master reset signal MRa corresponds to the master reset signal MR shown in Fig. 10, and it is applied to ~~junciton~~ junction unit JNC, C elements 2a to 2c and one input of OR gate 11a. Master reset signal MRb is input to program storing unit PS, host transfer flag operating circuit 10f and the other input of OR gate 11a. It is understood that OR gate 11a is included in ~~brnaching~~ branching unit BRN, as shown in Fig. 3.

Please replace the paragraph beginning at page 13, line 1 with the following new paragraph:

Host transfer flag detecting circuit 11e detects and latches the host transfer flag at the "H" level output from pipeline register 4d, and applies a signal at the "H" level to one input of each of the gate circuits 11b and 11c. A pulse signal is applied from the terminal CO of C element 2d to the other input of each of gate circuits 11b and 11c. An output of gate circuit 11b is applied to ~~junciton~~ junction unit JNC through terminal Ca, and an output of gate circuit 11c is applied to the outside (host) through terminal Cob. To the terminals RIa and Rib, transfer acknowledge signals are applied from the junction unit JNC and from the outside, respectively, and the transfer acknowledge signals are provided to the RI input of C element 2d through gate circuit 11d.

Please replace the paragraph beginning at page 13, line 12 with the following new paragraph:

In Figs. 2 and 3, the operation of host transfer flag operating circuit 10f is the same as described with reference to Fig. 1. When the dead-lock state occurs because of data dependency or lag in the timing of arrival of the data packets, the master reset signal MRb is set to the "H" level. Thus, the master reset signals MRa and MRb are input to the MR input terminal of C element 2d through OR gate 11a, and the data packet stored in pipeline register 4d in ~~brnaching~~ branching unit BRN is overwritten and eliminated.

Please replace the paragraph beginning at page 13, line 19 with the following new paragraph:

Thereafter, master reset signal MRb is set to the "L" level. Thus, the data packet stored in the pipeline register 4d in ~~brnaching~~ branching unit BRN is overwritten and eliminated, and a data packet having the host transfer flag at the "H" level is newly overwritten and stored in pipeline register 4d.

Please replace the paragraph beginning at page 13, line 33 with the following new paragraph:

As the data driven type information ~~procesisng~~ processing apparatus processes data by exchanging transfer request signals and

transfer acknowledge signals between C elements, the terminals COb and RIb correspond to the signals from the ~~otuside~~ outside (host), and hence, the data packet is transferred from the data driven type ~~informaiton proecessing~~ information processing apparatus. When the host transfer flag is at the "L" level, host transfer flag detecting circuit 11e latches and outputs the "L" level. At this time, gate circuit 11b is rendered active, and CO output of C element 2d is output from terminal COa. The terminals Coa and RIa exchange signals with junction unit JNC, and hence data packets are all returned to junction unit JNC. Host transfer flag detecting ~~ciruci~~ circuit 11e may have a simple structure such as a latch circuit or a simple delay circuit.

Please replace the paragraph beginning at page 14, line 12 with the following new paragraph:

Thus, the data packets are forcedly transmitted to the outside (host), and hence the dead-lock state is solved, and it becomes possible to debug the data on the circulation pipeline in the data driven type information processing apparatus on the outside (host). Generally, in a data driven type ~~informaiton~~ information processing apparatus, there are a plurality of data driven ~~tpe~~ type information ~~proecesisng~~ processing apparatuses PE such as shown in Fig. 10 connected through input/output control units (branching units and junction units) among which signals are

exchanged. The transfer to the host here means taking of a signal from the data driven type ~~informaiton~~ information processing apparatus to the outside.

Please replace the paragraph beginning at page 14, line 30 with the following new paragraph:

Here, once the master reset signal MRb attains to the "H" level, the output of the D type flip-flop is maintained at the "H" level even when the master reset signal return to the "L" level thereafter. Thus, the host transfer flag of the data packet transferred and stored in pipeline register 4c thereafter can be set to the "H" level. Only one host transfer flag operating circuit 10f have to be provided in the input stage of pipeline register 4d as the input stage of branching unit BRN, and therefore, the number of host transfer flag operating ~~cirucits~~ circuits to be provided can be reduced.

Please replace the paragraph beginning at page 15, line 16 with the following new paragraph:

By contrast, in the embodiment shown in Fig. 4, when the master reset signal MRb as the control signal is at the "L" level, host transfer flag operating circuit 2h stores this state, and it does not ~~ceprate~~ operate the host transfer flag of any packet input from pipeline register 1b thereafter, but outputs the packet

as it is to pipeline register 1c. Here, the host transfer flag is at the initial state of "L" level.

Please replace the paragraph beginning at page 16, line 17 with the following new paragraph:

Thereafter, the master reset signal MRb is set to the "L" level. Thus, the data packet stored in the pipeline register of the data transmission path in the branching unit BRN is overwritten and eliminated as already described, and as the host transfer flag of the overwritten data packet is at the "H" level, transfer to the ~~ouside~~ outside is enabled, dissolving the dead-lock state of the circulation pipeline.

Please replace the paragraph beginning at page 16, line 23 with the following new paragraph:

When the dead-lock state is dissolved, data packet transfer on the circulation pipeline restarts. When a data packet passes through the program storing unit PS nearest to the branching unit BRN, the host transfer flag of the data packet that is being passed and processed is set to the "H" level, by the "H" level signal stored in host transfer flag operating circuit 2h provided in program storing unit PS. In this example, in addition to the effects of the invention attained by the embodiment and modification described above, degree of freedom in debugging can be

~~icnreased~~increased, as additional adjustment of operation by the ~~cahnge~~change of a software is possible, as the host transfer flag operating circuit 2h is included in the program storing unit PS.

Please replace the paragraph beginning at page 17, line 16 with the following new paragraph:

As described above, according to the embodiments of the present invention, a function is provided that erases a data packet stored in a pipeline register and outputs other data packets to the outside. Therefore, the dead-lock state of a circulation pipeline can be dissolved and, in addition, other data packet on the circulation pipeline can be transferred to an external host. Thus, information of the data packet that is the cause of the dead-lock state can be easily obtained, and thus a data driven type information ~~procesisng~~processing apparatus having an effective debugging function can be realized.